Cadence OrCAD FPGA System Planner

FPGA-PCB co-design with automated "device-rules-accurate" pin assignment

The Cadence® OrCAD® FPGA System Planner addresses the challenges that engineers encounter when designing large-pin-count FPGAs on the PCB board—which includes creating the initial pin assignment, integrating with the schematic, and ensuring that the device is routable on the board. By replacing manual, error-prone processes with automatic pin assignment synthesis, this unique placement-aware solution eliminates unnecessary physical design iterations while shortening the time required to create optimum pin assignment.

Designing large-pin-count FPGAs on PCBs

Integrating today's FPGAs—with their many different types of assignment rules and user-configurable pins—on PCBs is time consuming and extends design cycles. Often the pin assignment for these FPGAs is done manually at a pin-by-pin level in an environment that is unaware of the placement of critical PCB components that are connected to FPGAs. Without understanding the impact to PCB routing, FPGA-based design projects are forced to choose between two poor options: live with suboptimal pin assignment, which can increase the number of layers on a PCB design; or deal with several unnecessary iterations at the tail end of the design cycle. Even with several iterations, this manual and error-prone approach can result in unnecessary PCB design re-spins.

With the added time required to generate pin assignments for FPGAs using manual approaches, users are unable to do trade-offs between the different FPGA devices available and the cost of devices used in an FPGA sub-system. This is because performing the trade-offs would mean that users would have to do two projects in parallel with no design reuse of any kind between the two.

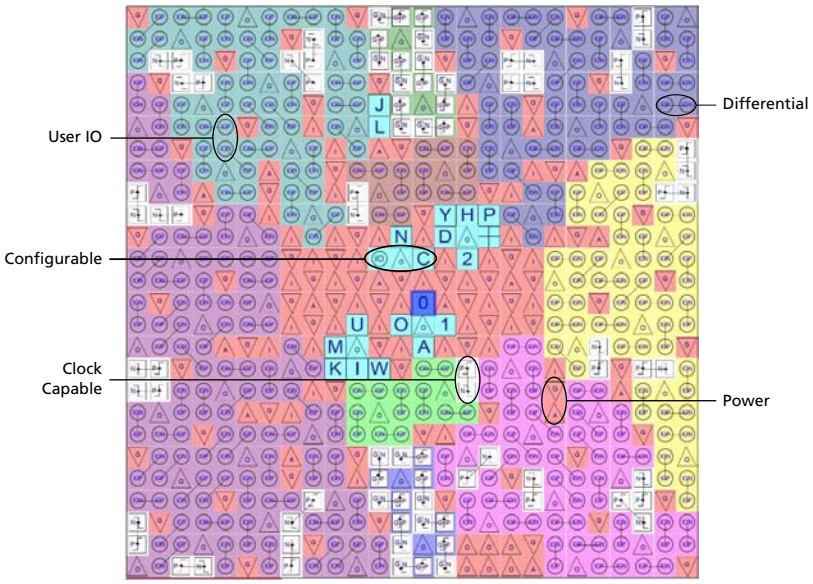

Figure 1: Color-coded map of the I/Os of a multi-bank FPGA with different types of configurable pins

The Cadence OrCAD FPGA System Planner provides a complete, scalable solution for FPGA-PCB co-design that allows users to create an optimum correct-by-construction pin assignment. FPGA pin assignment is synthesized automatically based on user-specified, interface-based connectivity (design intent), as well as FPGA pin assignment rules (FPGA-rules), and actual placement of FPGAs on PCB (relative placement). With automatic pin assignment synthesis, users avoid manual error-prone processes while shortening the time to

create initial pin assignment that accounts for FPGA placement on the PCB (placement-aware pin assignment synthesis). This unique placement-aware pin assignment approach eliminates unnecessary physical design iterations that are inherent in manual approaches.

The OrCAD FPGA System Planner is integrated with both OrCAD Capture and OrCAD PCB Editor. It reads and creates Capture schematics and symbols. In addition, a floorplan view uses existing footprint libraries from OrCAD PCB Editor. Should placement change during layout, pin optimization using FPGA System Planner can be accessed directly from OrCAD PCB Editor.

Benefits

- Scalable, cost-effective FPGA-PCB co-design solution from OrCAD to Allegro® GXL
- Shortens time for optimum initial pin assignment, accelerating PCB design schedules
- Accelerates integration of FPGAs with OrCAD PCB design creation environments
- Eliminates unnecessary, frustrating design iterations during the PCB layout process
- Eliminates unnecessary physical prototype iterations due to FPGA pin assignment errors
- Reduces PCB layer count through placement aware pin assignment and optimization

Features

OrCAD FPGA System Planner Technology

An FPGA system is defined as a subset of the PCB design that includes one or more FPGA and non-FPGA components that are connected to FPGAs.

Traditional approaches to pin assignment are typically manual and often based on a spreadsheet. Tools such as these require users to do pin assignment without taking into consideration the placement of other components and routability of the interfaces and signals. Above

Figure 2: Placement/Floorplan view of the OrCAD FPGA System Planner provides users relative placement of critical components for optimum pin assignment synthesis

all, there is no online rules-checking to ensure that the right pin types are being used for the signals that are assigned to the FPGA pins. As a result, users have to make several iterations between the spreadsheet-based tools and the tools from FPGA vendors. Often this adds an increased number of iterations between the PCB layout designer who cannot route the signals from FPGA pins on available layers and the FPGA designer who has to accept paper-based or verbal pin-assignment suggestions from the PCB layout designer. Once a change is made to the pin assignment by the FPGA designer, the pin assignment change has to be made in the schematic design by the hardware designer. Such iterations add several days if not weeks to the design cycle and possibly a great deal of frustration for the team members. Since this is a manual process, mistakes that are not detected can also cause expensive physical prototype iterations.

While it may help to automate the synchronization of changes made to the pin assignment by the FPGA designer, hardware designer, or PCB layout designer, it doesn't reduce the root cause of these iterations. Pin assignment that is not guided by all three aspects—FPGA resource availability, FPGA vendor pin assignment rules, and routability of FPGA pins on a PCB—requires many iterations at the tail end of the design process, thereby extending the time it takes to integrate today's complex, large-pin-count FPGAs on a PCB.

Specifying Design Intent

The OrCAD FPGA System Planner comes with an FPGA device library to help with selection of devices to be placed. It uses OrCAD PCB Editor footprints for the floorplan view and allows users to quickly create relative placement of the FPGA system components.

The OrCAD FPGA System Planner allows users to specify connectivity between components within the FPGA sub-system at a higher level through interface definitions. Users can create interfaces such as DDR2, DDR3, and PCI Express, and use these to specify connectivity between an FPGA and a memory DIMM module or between two FPGAs. The OrCAD FPGA System Planner understands differential signals, and power signals, as well as clock signals.

FPGA Device Rules

The OrCAD FPGA System Planner comes with a library of device-accurate FPGA models that incorporate pin assignment rules and electrical rules specified by FPGA device vendors. These FPGA models are used by the synthesis engine to ensure that the vendor-defined electrical usage rules of the FPGAs are strictly adhered to. These rules dictate such things as clock

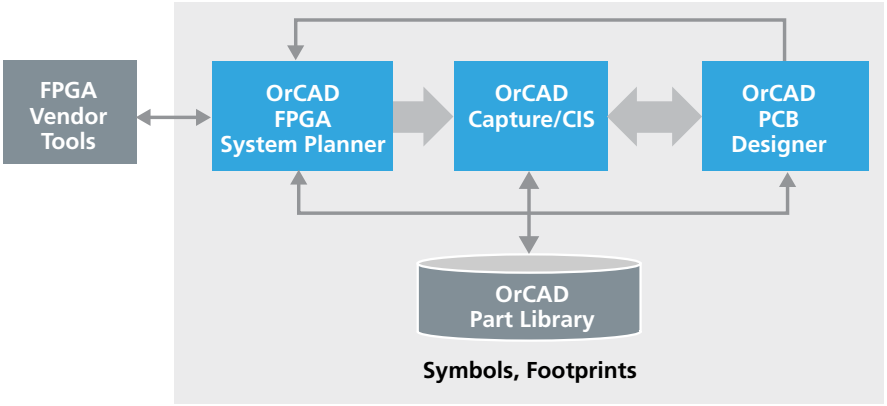

Figure 3: The OrCAD FPGA System Planner uses symbols and footprints from existing libraries

and clock region selection, bank allocation, SSO budgeting, buffer driver utilization, I/O standard voltage reference levels, etc. During synthesis, the OrCAD FPGA System Planner automatically checks hundreds of combinations of these rules to ensure that the FPGA pins are optimally and accurately utilized.

Placement Aware Pin Assignment Synthesis

The OrCAD FPGA System Planner provides users a way to create an FPGA system placement view using OrCAD PCB footprints. Users specify connectivity between components in the placement view and the FPGA at a high level using interfaces such as DDRx, PCI Express, SATA, Front Side Bus, etc. that connect FPGAs and other components in the design, shortening the time to specify design intent for the FPGA system.

Once the connectivity of the FPGA to other components in the sub-system is defined, the OrCAD FPGA System Planner then synthesizes the pin assignment based on the user's design intent, available FPGA resources, component placement around the FPGA, and the FPGA vendor's pin assignment rules.

The OrCAD FPGA System Planner has a built-in DRC engine that incorporates the rules provided by FPGA vendors for pin assignment, reference voltages, and terminations. This rules-based engine prevents PCB physical prototype iterations as the FPGAs are always correctly connected.

Pin assignment algorithms are optimized to assign interface signals to a group of pins, thereby minimizing net crossovers and improving routability on the PCB.

Tight Integration with Cadence Design Creation

The OrCAD FPGA System Planner generates OrCAD Capture, schematics for the FPGA sub-system. It uses existing symbols for FPGA in OrCAD Capture symbol libraries. If the user desires, the FPGA System Planner products can create split symbols for FPGA based on the connectivity or one split symbol per bank.

Integration with FPGA Vendor Tools

In addition to integration with OrCAD PCB design tools, the OrCAD FPGA System Planner communicates seamlessly with FPGA design tools. It generates and reads supported FPGA vendors' pin assignment constraint files. This capability enables the FPGA designer to evaluate pin assignments against the functional needs of the FPGA. Any changes made by the FPGA designer to account for these requirements can be imported into to the OrCAD FPGA System Planner so that the complete set of pin assignments remain in sync.

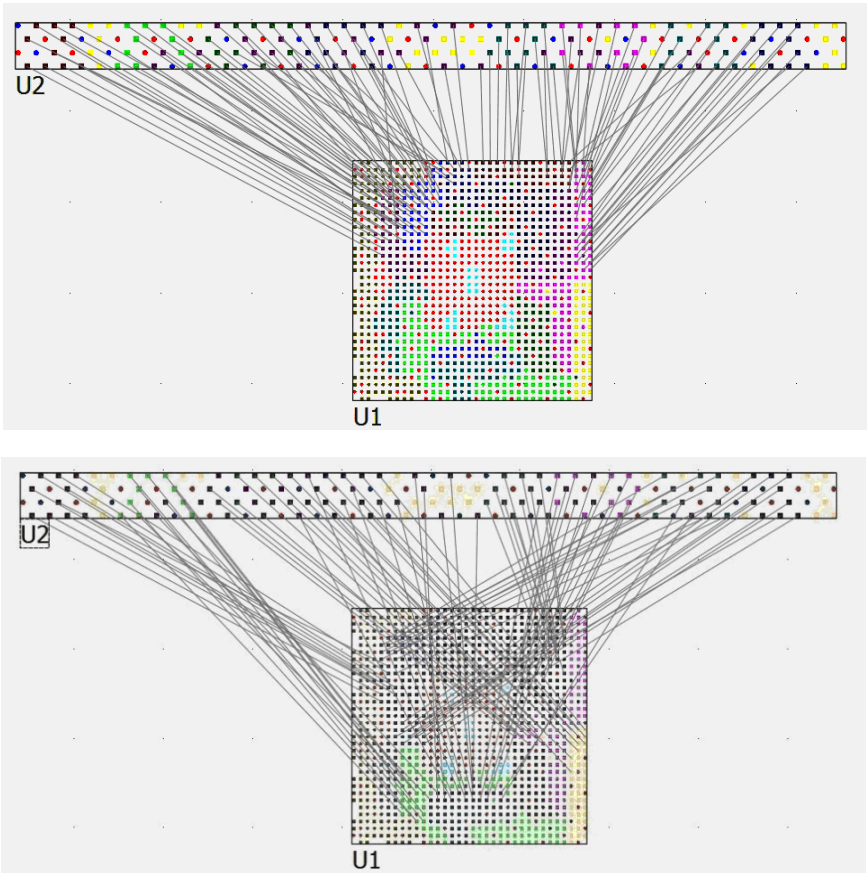

Figure 4: OrCAD FPGA System Planner optimization

Pre-Route Pin Assignment Optimization

The initial pin assignment—that accounts for placement and routability of the FPGA on a PCB—goes a long way toward reducing costly design iterations between FPGA designer, PCB layout designer, and hardware designer. Once the PCB layout designer starts to plan the routing of interfaces and signals on FPGA, it is possible to further refine the FPGA pin assignment based on route intent, layer constraints, and fanout chosen for the FPGA. The OrCAD FPGA System Planner offers users a way to optimize FPGA pin assignment after placement and during routing of the interfaces and signals on an FPGA.

Scalability

The OrCAD and Allegro FPGA System Planner technology is available in the following product offerings:

- Allegro FPGA System Planner GXL—for synthesizing and optimizing pin assignment of more than four FPGAs at a time. Suitable for companies that use FPGAs to prototype ASICs
- Allegro FPGA System Planner XL—for concurrent pin assignment, synthesis, and post-placement optimization of up to four FPGAs at a time
- Allegro FPGA System Planner L—for pin assignment synthesis and post-placement optimization of a single FPGA
- OrCAD FPGA System Planner—for optimum initial pin assignment synthesis of a single FPGA.

Sales, Technical Support, and Training

The OrCAD product line is owned by Cadence Design Systems, Inc., and supported by a worldwide network of Cadence Channel Partners (VARs). For sales, technical support, or training, contact your local Cadence Channel Partner. For a complete list of authorized Cadence Channel Partners, visit www.cadence.com/Alliances/channel_partner.

	OrCAD FPGA System Planner	Allegro 2 FPGA System Planner Option	Allegro 4 FPGA System Planner Option	Allegro ASIC Prototyping Option
Concurrent device optimization	1 FPGA or Multiple FPGAs totaling 1,000 max pins	2 FPGAs or Multiple FPGAs totaling 2,000 max pins	4 FPGAs or Multiple FPGAs totaling 4,000 max pins	Unlimited FPGAs
Placement-aware synthesis	Yes	Yes	Yes	Yes
Reuse symbols and footprints	Yes	Yes	Yes	Yes
Symbols and schematic generation	OrCAD Capture	Allegro Design Entry CIS / Allegro Design Entry HDL	Allegro Design Entry CIS / Allegro Design Entry HDL	Allegro Design Entry CIS / Allegro Design Entry HDL
Post-placement optimization	No	Yes	Yes	Yes
Schematic power connections	No	Yes	Yes	Yes

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