

Cadence Sigrity OptimizePI

Cost-based power-delivery system design

The Cadence® Sigrity™ OptimizePI™ environment automates the selection and placement of decoupling capacitors (decaps) to assure products meet power delivery system (PDS) performance targets at the lowest possible cost. The OptimizePI approach may be applied to PCBs and IC packages, or a combination thereof. Cadence Sigrity's proprietary and proven analysis technologies are augmented with an efficient optimization engine to uniquely enable cost-based PDS design. OptimizePI capabilities can fully explore the feasible design space and identify a range of candidate decap implementations, enabling users to pinpoint the ideal approach.

Benefits

Use OptimizePI to:

- Automate the selection and placement of decaps
- Eliminate decap over-design for PCBs and IC packages
- Reduce PDS cost of new designs and postproduction products
- Recapture design area used by unnecessary decaps
- Develop effective decap design guidelines
- Investigate pre-layout decap placement and selection scenarios
- Interactively assess trade-offs for PDS cost vs. performance
- Understand both system- and device-level PDS performance
- Create lowest-cost, best-performance decap placement tables

Unprecedented Cost Savings

Eliminate decap over-design

Decap cost savings of 15% to 50% are typical with the OptimizePI environment. Designs with a large number of decap components and those manufactured in volume benefit most. Cost savings are achieved by reducing the number of decaps placed and by targeting lower-priced components where practical. Device suppliers may suggest general guidelines such as “one decap per power pin” or describe

preferred decap implementation schemes. Both approaches typically lead to an overly robust system. The OptimizePI approach helps companies capitalize on this margin to gain market advantage.

Assure PDS performance

OptimizePI cost savings are achieved while analytically assuring PDS performance. Alternatively, OptimizePI may be configured to maximize performance or reduce decap area without regard for cost. Complex inter-

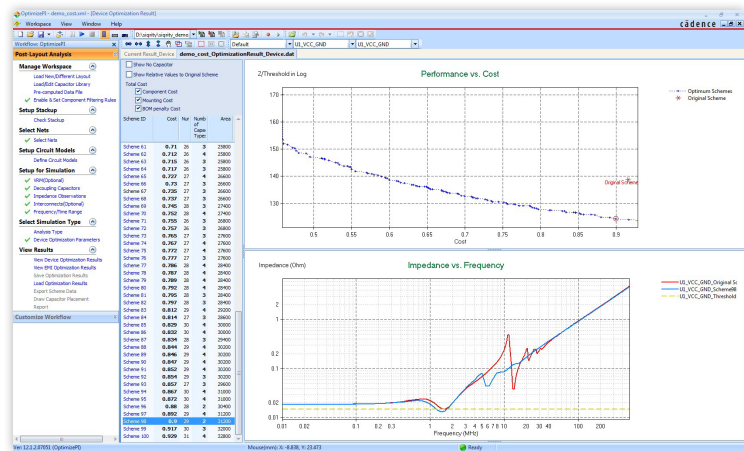


Figure 1: OptimizePI capabilities quickly pinpoint designs that offer the same or better performance at lower cost

actions among performance, decap selection, component cost, and placement expense are considered. The OptimizePI design schemes are the best-performing alternatives from all feasible designs. Analysis results are based on aggregate PDS performance averaged across frequency. Users can set device-specific targets and identify critical frequencies for further refinement. Time-domain results confirmation is also included.

Use Model

While primarily targeting post-layout PDS optimization, pre-layout design scenarios can also be explored. This helps to eliminate decap over-design earlier in the design flow and supports development of analytically based decap placement design guides for individual devices. For post-layout applications, the OptimizePI approach works from an initial design imported from a layout database. OptimizePI capabilities can also be applied by manufacturing engineers for postproduction cost reduction.

Task-Focused workflow

Setting up a design in the OptimizePI environment typically requires less than 30 minutes of engineering time. Users are guided step by step through each task in the workflow. Initial set-up involves importing the PCB or IC package design and identification of an OptimizePI library corresponding to a corporate decap preferred parts list. Decap component and placement costs are included in this library along with vendor-supplied electrical models. Set-up options enable decap selection filtering, biasing the importance

of a device to overall PDS performance, and so on. Individual decap selections may be limited to a subset of the library or restricted by decap size. An interactive results window enables exploration of alternate design schemes. OptimizePI results can be exported to a spreadsheet for back annotation to the layout system.

Integration

- Works with Microsoft Windows and Linux with multi-processor support
- Interfaces to PCB and IC package layout databases from Sigrity, Cadence, Mentor Graphics, Altium, Zuken, etc.

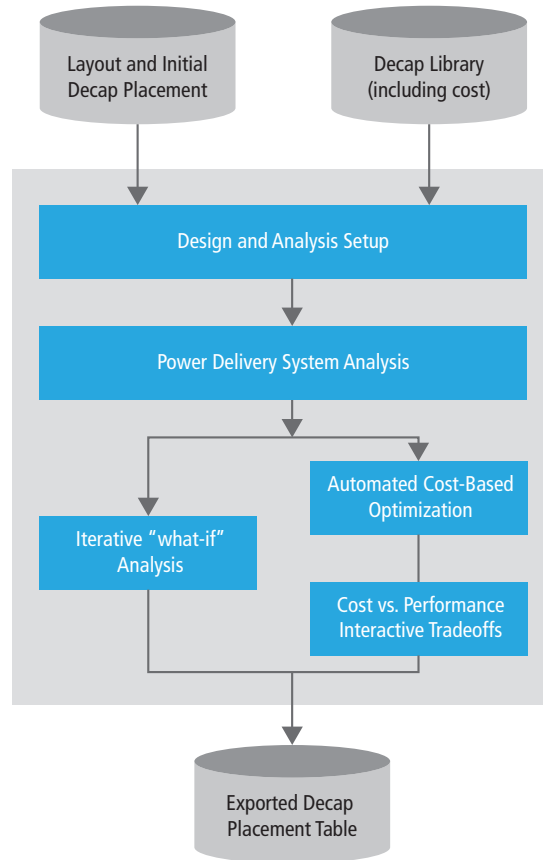


Figure 2: OptimizePI workflow for a post-layout optimization