cadence® OrCAD™
CADENCE EDA SOLUTIONS

OrCAD & Allegro V17.2 - 2016

Features comparison

Feature	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
• SCHEMATIC ENTRY + DATA MANAGEMENT			
Graphical, flat and hierarchical page editor and Picture block hierarchy	•	•	•
Unlimited undo/redo	•	•	•
Net Groups - Complex bus definition	•	•	•
Intelligent PDF creation	•	•	•
AutoWire	•	•	•
Design reuse	•	•	•
3D Footprint Viewer	•	•	•
Coloured Components / nets	•	•	•
Tcl scripting customization	•	•	•
Online design rule check including custom DRC capability and Waive DRC	•	•	•
PCB Forward and back-annotation of properties / pin-and-gate swaps	•	•	•
Schematic Part and Library editor	•	•	•
Cross-probing and cross-placement	•	•	•
FPGA design-in / pin import & export and FPGA bi-directional support	•	•	•
Multiple PCB netlist interfaces	•	•	•
SI Topology creation	•	•	•
Digi-Key (PartLink App) Component Parametric data directly from web	•	•	•
Property editor for pins, components, nets	•	•	•

• Included function

Feature	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
Design differences viewer	•	•	•
Intelligent PDF creation	•	•	•
Component Information System			
Centralized part information system	CIS option	CIS option	•
Relational data support	CIS option	CIS option	•
ODBC-compliant database support	CIS option	CIS option	•
Graphical preview of database parts	CIS option	CIS option	•
Intelligent database query	CIS option	CIS option	•
Component property validation	CIS option	CIS option	•
Interface to relational database and management systems	CIS option	CIS option	•
Database query for part selection and parametric properties	CIS option	CIS option	•
Extensive reports and report templates	CIS option	CIS option	•
Crystal Reports™ for advanced documentation	CIS option	CIS option	•
Unlimited assembly variant support	CIS option	CIS option	•
Schematic and BOM Variants Manager (Parts not Fitted and more).	CIS option	CIS option	•
CIS Database Management Interface (access control and more)	CIS Option + CIP E Option	CIS Option + CIP E Option	CIP E Option
Part search DIGIKEY, FARNELL, FUTURE, MOUSER, ARROW	CIS option	CIS option	CIS option
Import			
PSpice schematic, EDIF, PDIF, XML	•	•	•
PADS schematic design	•	•	•
Import Altium schematic design	•	•	•
Import Eagle schematic design	•	•	•
Export			
PDF, DXF,EDIF, XML, ISCF	•	•	•
• PCB EDITOR			
Library			
Padstacks			
9 standard shapes including rounded rect, chamferred rect, donut	•	•	•
User defined shapes (flash)	•	•	•
Adjacent Layer Keepout	•	•	•

• Included function

Feature	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
Finished drill size	•	•	•
Actual drill size	•	•	•
Backdrill size and clearance support	•	•	•
Counter bore/sink objects	•	•	•
(32) User defined layers (non conductor)	•	•	•
Bond fingers	•	•	•
Die Pads	•	•	•
Package Symbols			
Symbol wizard	•	•	•
Placebound shape	•	•	•
DFA placebound shape	•	•	•
No probe area	•	•	•
Constraint region shape	•	•	•
Built-in fanout vias	•	•	•
Associated copper/keepouts	•	•	•
STEP model mapping	•	•	•
Associative dimensioning	•	•	•
Additional Symbols			
Mechanical	•	•	•
Format	•	•	•
Shape	•	•	•
Flash	•	•	•

Import			
IPC-2581	•	•	•
IPC-2581 xSection (from PCB Vendors)	•	•	•
IPF	•	•	•
DXF	•	•	•
IDF	•	•	•
IDX	•	•	•
Stream (GDSII)			•
RF IFF	•	•	•
Router	•	•	•
Translators:			
Mentor Boardstation			•
CadSoft Eagle	•	•	•

• Included function

Feature	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
PADS	•	•	•
PADS Library	•	•	•
PCAD	•	•	•
Altium PCB	•	•	•
Altium SCH - DE HDL	•	•	•
Placement			
Place application mode	•	•	•
Flow planning application mode			•
Cross probe to schematic	•	•	•
3D visualization / flipboard	•	•	•
Quickplace utility	•	•	•
Component alignment	•	•	•
Place by room / by schematic page	•	•	•
Placement replication		•	•
Native 3D viewer (STEP & Simple Extrusions)	•	•	•
Floorplanning, autoplace	•	•	•
Dynamic DFA rules based interactive placement			•
Component height checks	•	•	•
Routing			
Etch edit app mode	•	•	•
Interactive routing	•	•	•
Scribble route	•	•	•
Group routing (Multi-line routing)	•	•	•
Diff pair routing	•	•	•
Snake routing (Hex pitch BGA)	•	•	•
Contour Routing - Flex		•	•
Jumper support (Single-sided design)	•	•	•
Slide/Split stacked vias	•	•	•
Fan-out generators	•	•	•
Copy fanout to same packages	•	•	•
Interactive delay tuning		•	•
Phase tune bumps			•
Dynamic heads-up display		•	•
Single click multiple hdi-via instantiation	•	•	•

• Included function

Feature	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
Shape based curve fillet support, tapered traces		•	•
Resize/Respace diff pairs			•
Spread Lines between Anti-pads		•	•
Segment over void detection		•	•
Dynamic ratnest suppression during Routing	•	•	•
Auto-Interactive Routing (AiXX)			
Auto-connect router			Design Planning Option
Delay tune			High Speed Option
Phase tune			High Speed Option
Remove tuning			High Speed Option
Breakout			Design Planning Option
Trunk router			Design Planning Option
Convert corner			•
Create flow/autoroute			Design Planning Option
Adjust spacing			Design Planning Option
Autorouting			
6 signal layers at a time (no plane layer limit or pin limit)		•	•
Shape-based or gridded routing		•	•
SMD fanout		•	•
Trace width by net and net classes		•	•
45-degree / Memory pattern routing		•	•
Interactive routing with shoving and plowing		•	•
Interactive floorplanning		•	•
Online design rule checking		•	•
Flip, rotate, align, push, and move components		•	•
Placement density analysis		•	•
High speed rules based autorouting			SPECCTRA_HP
Min/Max, matched length rules based autorouting			SPECCTRA_HP
Pin-pair rules, area rules based autorouting			SPECCTRA_HP
Crosstalk controls, parallelism rules based autorouting			SPECCTRA_HP

• *Included function*

Feature	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
Differential pair autorouting, automatic net shielding			SPECCTRA_ performance
High-speed rules-based autorouting			SPECCTRA_HP
256 signal layer limit		OrCAD Router Auto/Interactive Option	SPECCTRA_256U
DFM rules-based autorouting			SPECCTRA_ autoroute
Automatic trace spreading		•	•
ATP generation		•	•
Layer-specific rules-based autorouting			SPECCTRA_ performance
High-Speed rules based autorouting			SPECCTRA_HP
Shapes (Copper Pour)			
Shape edit application mode	•	•	•
Z-Copy (expand, contract, change layers)	•	•	•
Intelligent planes	•	•	•
Dynamic copper (solid, cross-hatched)	•	•	•
Dynamic shapes with real-time plowing & healing	•	•	•
Static copper (solid, cross-hatched)	•	•	•
Boolean options (AND, OR, ANDNOT)	•	•	•
Merge shapes	•	•	•
Pin/Via thermal/clearance settings by layer	•	•	•
Auto chamfering/rounding of corners	•	•	•
Shape transparancy levels	•	•	•
Split Plane (negative planes)	•	•	•
Online DRC Checks			
Mutli-core/threaded DRC	•	•	•
Window DRC	•	•	•
Waive & restore DRCs	•	•	•
Heads-up display -electrical constraint adherence		•	•
DFM DRCs			
Acute angle	•	•	•
Negative plane sliver	•	•	•
Negative plane islands	•	•	•
Soldermask-soldermask	•	•	•

• Included function

Feature	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
Solderpaste-solderpaste	•	•	•
Testpoint to component	•	•	•
Duplicate drill	•	•	•
Drill to drill	•	•	•
Drill to metal	•	•	•
Minimum metal to metal	•	•	•
Constraint Manager:			
Physical rules	•	•	•
Spacing rules	•	•	•
SameNet rules	•	•	•
Properties and DRCs	•	•	•
Differential pairs and static phase control	•	•	•
Differential pairs dynamic phase control			•
Region rules		•	•
Single line impedance rules		•	•
Min. / Max. propagation rules		•	•
Relative propagation rules		•	•
Layer set rules		•	•
Electrical constraint rule set (ECSets) / topology apply		•	•
Matched group rules		•	•
Advanced constraints (formulas, relational)			•
Electrical rules (reflection, timing, crosstalk)			•
Package pin delay (for die-2-die delay) rules			•
Z-Axis delay feedback			•
Total etch length	•	•	•

Simulation			
Signal Integrity			
Graphical topology definition and exploration	•	•	•
Interactive waveform viewer	•	•	•
OrCAD Capture SI integration and flow	•	•	•
Macro modeling support (DML)	•	•	•
IBIS 5.0 and ICM model support	•	•	•
Spectre®-to-DML and HSpice-to-IBIS conversion	•	•	•

• Included function

Feature	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
Lossy transmission lines	•	•	•
Coupled (3 net) simulation	•	•	•
Differential-pair exploration and simulation	•	•	•
Single net extraction from PCB Editor		•	•
Post- route signal integrity analysis		•	•
Co-design			
Swap pins on a FPGA (based on FPGA rules) in PCB Editor			FPGA System Planner option
Re-optimize pins on a FPGA (using FPGA rules)			FPGA System Planner option
Design Intelligence			
Command snapping to object	•	•	•
Undo/Redo	•	•	•
Constraint regions		•	•
Region rules by layer		•	•
TimingVision advanced timing closure engine			High Speed Option
Extended net (X-Nets) creation		•	•
Via Array placement on traces, shapes		•	•
F2B reuse modules			•
Design Planning:			
Create hierarchical bundles			Design Planning Option
Create, edit flows			Design Planning Option
Assign flows to layers			Design Planning Option
Plan spatial feasibility analysis & feedback			Design Planning Option
Generate topological plan			Design Planning Option
Convert topological plan to traces (CLINES)			Design Planning Option
Design Units:			
Mils	•	•	•
Inch	•	•	•
Microns	•	•	•
Millimeter	•	•	•
Centimeter	•	•	•

• Included function

Feature	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
Advanced Technologies			
Rigid-Flex			
Cross section by zone		•	•
Cross section support for mask/coating Layers	•	•	•
Inter layer DRC (mask to mask; mask to surface conductor)		•	•
Zone table chart for manufacturing		•	•
Dynamic zone placement (auto drop down)		•	•
Native database flex and surface finish layers	•	•	•
Techfile support of zones		•	•
Curved fillets		•	•
Auto-rounding shape corners	•	•	•
Dynamic cross hatch and solid planes	•	•	•
Contour routing wihile shoving arc routes			•
IDX support of zones (Siemens only)	•	•	•
High Density Interconnect (HDI)			
Microvia database element			Miniaturization Option
Microvia to microvia/buried via spacing rules			Miniaturization Option
Stacked microvia DRC			Miniaturization Option
Stacked, staggered, inset via patterns	•	•	•
Tangent HDI via line fattening	•	•	•
Stacked via labels	•	•	•
Removal of unused vias in stack			•
Via in pad fanout and DRC	•	•	•
Fanout with predefined via structures	•	•	•
Blind / Buried microvia stacking, split, & merge support	•	•	•
Replace thru via with stacked via	•	•	•
Embedded Component Design			
Embedded component direct/indirect attachment			Miniaturization Option
Dynamic cavities			Miniaturization Option
Max cavity size DRC			Miniaturization Option
Max component count in cavity			Miniaturization Option
Protrusion through adjacent layers			Miniaturization Option

• Included function

Feature	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
Cavity height checks			Miniaturization Option
Advanced High Speed Interconnect			
Tabbed routing (Intel)			High Speed Option
High speed differential pair via structures (Sigrity Integration)			High Speed Option
Fabric weave routing			High Speed Option
Diff pair return path via templates			High Speed Option
Single net return path via templates			High Speed Option
RF and Analog Design			
Parameterized RF etch elements			PCB RF Option
RF Etch elements editing			PCB RF Option
Layout-driven RF design creation			PCB RF Option
Asymettrical clearances			PCB RF Option
Flexible shape editor			PCB RF Option
Bi-Directional interface with Agilent ADS			PCB RF Option
Bi-Directional interface with AWR			PCB RF Option

Manufacturing Prep			
Customizable, automated drill legend / NC output	•	•	•
Auto testpoint insertion (vias, pins. traces)		•	•
Testability (multi probe setup)	•	•	•
Testability (density checks)	•	•	•
Dynamic unused pad suppression	•	•	•
Any layer thieving	•	•	•
Associative dimensioning	•	•	•
Drafting suite (trim, extend, offset)	•	•	•
Auto silkscreen	•	•	•
Backdrilling (library or parameter driven)			•
Separate backdrilling NC files			•
Separate zone stackup charts		•	•

Export			
Gerber 274X, 274D	•	•	•
IPC-2581	•	•	•
IPF	•	•	•

• Included function

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DXF	•	•	•
IDF	•	•	•
IDX	•	•	•
RF IFF	•	•	•
STEP	•	•	•
Router	•	•	•
IPC-356	•	•	•
FABMaster	•	•	•
ODB++	•	•	•
Creo View	•	•	•
HTML-based reports	•	•	•
Assembly variant	•	•	•
Variant BOMs	•	•	•

Team Design			
Design Partitioning			
Zone restricted team design environment			Allegro PCB Team Design Option
Vertical and horizontal partition definitions			Allegro PCB Team Design Option
Soft nets and boundaries			Allegro PCB Team Design Option
Constraint editing in partitions			Allegro PCB Team Design Option
Concurrent Team Design:			
Real time collaborative design environment			Concurrent Team Design Option
Structure- LAN			Concurrent Team Design Option
Max users - 5			Concurrent Team Design Option
Interactive routing			Concurrent Team Design Option
AiDT and AIPT			Concurrent Team Design Option
Component move			Concurrent Team Design Option

• *Included function*

Feature	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
Extensibility / Open Architecture			
64-Bit architecture	•	•	•
SKILL extension language	•	•	•
Database extraction (Extracta)	•	•	•
Scripting	•	•	•
Menu customization	•	•	•
Datatip customization	•	•	•
Toolbar customization	•	•	•
Design save without IP	•	•	•
Lockable design file	•	•	•
Technology file compare	•	•	•

• *Included function*

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