cādence®

Allegro Design Authoring
Create design intent with ease for simple to complex designs

Systems companies looking to create new products at the lowest possible cost need a way to author their designs with ease in a shorter, more predictable design cycle. With the increased use of new standards-based interfaces, architectures, and implementation approaches, hardware designers require a design authoring solution that scales with their evolving technology and methodology needs. Cadence® Allegro® Design Authoring is a scalable and easy-to-use solution for fast design intent creation (connectivity plus high-speed constraints) using either schematics or a spreadsheet-like interface.

Allegro Design Authoring

Available in "base plus options" configurations, Allegro Design Authoring provides a scalable solution that adapts to your changing needs. Allegro Design Authoring (Base) provides a robust, yet easy-to-use schematic creation environment that allows you to create flat or hierarchical schematics for your products. Its enterprise-ready Schematic Editor integrates seamlessly with Allegro AMS Simulator, Allegro PCB SI Signal Explorer and Simulator, and Allegro PCB Designer, enabling a constraint-driven PCB design flow for predictable digital, analog, RF, and mixed-signal designs.

The Multi-Style Option allows you to create connectivity for your designs very quickly without requiring symbols or having to graphically connect pins/ports on symbols. Its spreadsheet-like interface makes it easy to create design intent for large pin-count devices or backplane designs 5x to 20x faster than traditional schematic-based approaches. The High-Speed Option allows you to create true design intent by integrating high-speed constraints with the connectivity through hierarchical, reusable electrical con-

straint sets (ECSets). This enables a constraint-driven PCB implementation flow to ensure a shorter, predictable, and complete PCB design cycle from concept to manufacturing.

Other configurations include a Team Design Option, an FPGA System Planner Option, an FPGA ASIC Prototyping Option, and a Design Publisher Option.

Benefits

- Shortens time to create design intent

- Enables concurrent schematic and layout design

- Reduces design spins via a proven, constraint-driven flow

- Reduces rework and prevents errors by supporting flexible design reuse

- Eliminates rework with a single schematic that drives digital, analog, and pre-layout signal integrity simulators

- Reduces total cost of ownership through a scalable "base plus options" configuration that is enterprise deployment–ready

Features

Schematic Editing

Allegro Design Authoring maximizes workflow efficiencies through its collaborative design approach. The design can be partitioned at a sheet or block level, and each designer can be assigned one or more blocks or sheets. Any number of designers can work on different parts of the same design simultaneously without interfering with each other. The various design stages can then be combined before proceeding to layout in Allegro PCB Editor. This concurrent design approach makes Allegro Design Authoring extremely productive for large designs. Designers work on the board layout and schematic in parallel. Changes made in either Allegro Design Authoring or Allegro PCB Editor can be merged and synchronized periodically.

Schematic Editor within Allegro Design Authoring allows you to create flat or hierarchical designs without requiring you to enter into "hierarchical" or "occurrence" modes. It provides a cross-referencer that annotates the schematic with references to allow easy tracking of signals on plotted

schematics. Schematic Editor also allows you to place multiple discrete components quickly. For example, to place 512 resistors that tie into a 512 bit bus, you need only place one resistor on the bus and specify that 512 such components need to be placed, and Schematic Editor will connect 512 bits to 512, greatly reducing the number of graphical components needing to be placed and displayed within a design.

The Allegro Design Authoring point-to-point wire router makes it easy to connect ports on two different symbols, saving time to create the schematics. Similarly, automatic insertion of a two-pin component within an existing net generates associated input and output pins automatically while adhering to the associated net names, shortening time to create basic schematics.

Whether you're using a flat design with a few hundred sheets or a hierarchical design with multiple levels of hierarchy, Global Navigate allows you to navigate to any net or part in your design with a few mouse clicks. The dock-able Global Find and Replace window allows you to find and replace parts or properties across the design. These can be highlighted directly from Allegro PCB Editor or Allegro PCB SI.

Customizable Rules Checking

Allegro Design Authoring eliminates multiple design iterations with Rules Checker, a truly comprehensive verification facility. It allows you to perform electrical and design rule checks to verify drafting standards and correct property names, syntax, and values. Rules Checker also includes rules to support downstream processing, fan-in and fan-out errors, load errors, power requirements, and cost requirements. Rules Checker checks the alignment between logical and physical designs. In addition, it lets you define custom rules to ensure conformity to design requirements specific to your company or your projects. Rules Checker can be used for schematics, symbols, and the physical netlists. It has a rule development and debugging environment for defining rules and can run in batch mode, facilitating deployment in an enterprise environment.

Design Reuse with Module Design

Most designs start from other designs or reuse significant parts of existing designs. Allegro Design Authoring gives you multiple choices for reuse, so you can select the most effective approach for their design. Sheets from old designs, blocks, or entire designs can be reused, which reduces rework and errors. You can copy single or multiple sheets from one design to another using the Import Sheet UI, or just copy/paste special circuitry among different designs. You can reuse electrical constraints as part of a block or by using electrical constraint sets (ECSets). The technology further allows you to create "reuse" blocks and place them in a library for use in other designs, just as with components. The connectivity, constraints, and layout from each block can also be reused. The same block can be used multiple times in the same design without renaming or copying.

FPGA Design-In

Allegro Design Authoring provides a comprehensive FPGA design-in solution. The Build Physical Wizard allows you to import Xilinx, Actel, and Altera FPGAs into your Allegro Design Authoring schematic and automatically creates the files required to drive Allegro PCB Editor, Allegro Design Authoring, and the digital simulation flow. Allegro Design Authoring also intelligently manages the interface to the FPGA so that the board schematic changes when the FPGA pin assignments change, but the design does not change logically.

FPGA-PCB Co-Design

Integrated with Allegro Design Authoring, Allegro FPGA System Planner provides a complete, scalable solution for FPGA-PCB co-design that allows you to create an optimum correct-by-construction pin assignment. FPGA pin assignment is synthesized automatically based on user-specified, interface-based connectivity (design intent), as well as FPGA pin assignment rules (FPGA rules), and actual placement of FPGAs on PCB (relative placement). With automatic pin assignment synthesis, you avoid manual error-prone processes while shortening the time to create initial pin assignment that accounts for FPGA placement on the PCB

(placement-aware pin assignment synthesis). This unique placement-aware pin assignment approach eliminates unnecessary physical design iterations that are inherent in manual approaches.

FPGA System Planner reads Allegro Design Authoring symbols and creates Allegro Design Authoring schematics. It also integrates with Allegro PCB Editor, from which it uses existing footprint libraries via a floorplan view. Should placement change during layout, pin optimization using FPGA System Planner can be accessed directly from Allegro PCB Editor.

Design Variants

By leveraging the design variants capability in Allegro Design Authoring, you can conserve even more time and effort at the structural level. The design variants capability eliminates having to create slightly different versions of the same basic design—for example, offering graduated performance levels to different market segments, or addressing varying regional requirements. It enables you to derive variants of a single base design by assigning alternate sets of attributes to the components, wires, or other elements of the design. An engineering change order (ECO) applied to the base design automatically propagates to all its variants.

Bill of Materials Generation

Allegro Design Authoring gives you fine-tuned control over bill of materials (BOM) creation, ensuring parts lists that meet your needs precisely and contain everything necessary for manufacturing. You can generate a BOM for a base design or any of its variants, list non-electrical parts in a callout file, and have Allegro Design Authoring merge them in the BOM with the electrical parts from the schematic. You can associate electrical and non-electrical parts in the schematic—for example, a heatsink with an IC—and have that association shown in the BOM. You can output the BOM in ASCII text, spreadsheet, or HTML format as needed to optimize transmission to manufacturing and other recipients.

PCB Editor Integration

The integration of Allegro Design Authoring with Allegro PCB Editor makes it the Schematic Editor of choice for all designers looking to increase productivity. The front-to-back flow automatically takes care of backannotation of pin, section, and component swapping in Allegro PCB Editor to Allegro Design Authoring schematics. Two-way cross-probing between Allegro PCB Editor and Allegro Design Authoring allows you to locate components in the schematic by highlighting the component in Allegro PCB Editor and vice versa.

To help in the placement phase, you can place components in Allegro PCB Editor by selecting the components in the Allegro Design Authoring schematic canvas. You can also place all components on an Allegro Design Authoring schematic page in a single step in Allegro PCB Editor. Using design differences, you can compare schematics and boards before transferring design information in either direction. With design association, you can backannotate terminators and bypass capacitors added directly to the board to the schematic. This allows logic design and signal integrity design to proceed in parallel. The Physical Viewer included with Allegro Design Authoring lets you view the Allegro PCB Editor. This is beneficial for viewing ECOs and other documentation-related issues.

Part Development

Allegro Design Authoring solution includes Part Developer, which enables creation and validation of symbols and part data. Part Developer provides a powerful mix of functionality that includes the ability to quickly enter and manipulate data, split pins across multiple symbols and define visibility for power and ground pins.

AMS Simulation

Allegro Design Authoring is tightly integrated with Allegro AMS Simulator 210 for fluid analog simulation. You can configure schematic symbols to reference Spice simulator models and simulate the design from within the Allegro Design Authoring environment. You can also cross-probe between schematic and simulation environments to quickly locate and characterize design bugs. This provides a reliable, low-cost analog simulation and verification solution for Allegro Design Authoring customers on the Windows platform. At the other end of the spectrum, Analog Workbench provides a high-end comprehensive analog design environment that is integrated with Allegro Design Authoring only on the UNIX platform.

High-Speed Design

Integration with Allegro Constraint Manager makes creating design intent quick and easy—it adds physical and electrical constraints that make communication of constraints reliable. Integrating constraints with schematic creation makes capturing and communicating design intent to downstream processes very efficient and eliminates the risk of unnecessary prototype iterations. It also shortens the PCB implementation process by enabling a constraint-driven PCB design flow.

The spreadsheet-like system allows you to capture all electrical constraints within the design database, eliminating the need to communicate constraints and design data separately. Advanced features include the ability to automatically extract, use, and override constraints from blocks added to the design.

Constraint Manager presents constraints through several separate worksheets for different types of electrical constraints. It allows you to capture, manage, and validate the different rules in a hierarchical fashion. Constraint Manager enables you to group all of the high-speed constraints for a collection of signals to form an electrical constraint set (ECSet). This ECSet is then associated with all the nets in the group. Constraint Manager is integrated with both Allegro Design Authoring and the physical design tools, making it easy to capture and manage constraints during the logical design phase. At any point during the design phase, you can launch Constraint Manager to add, view, and manage high-speed constraints in formation. As the rules are embedded in the design, the PCB layout designer can concentrate on optimizing the physical layout for size, routability, and manufacturability, while the software automatically communicates compliance with the engineer's performance requirements.

RF Circuit Design

Many of today's digital PCB systems include some circuitry that operates at radio frequencies. These blocks have special design requirements and are predominantly designed and simulated with Agilent ADS (formerly Agilent EEsof). However, this block needs to be present on the same board along with other digital and analog circuitry. To enable this, Allegro Design Authoring and Allegro PCB Editor provide a flow to import RF blocks designed in Agilent ADS into the Cadence board design flow.

Allegro PCB Editor and Allegro Design Authoring can automatically import the ADS physical layout and schematic through a robust interface. Once imported, the ADS design behaves like a module, with its components mapped to Allegro PCB Editor library parts. The imported module can be locked (to prevent editing) or unlocked (to allow editing). Even if locked, the module still allows you to connect it with the rest of the design and assign constraints to the nest connected to the block.

Multi-Style Design Creation

The Allegro Design Authoring Multi-Style Option helps you create design intent for complex PCBs faster by letting you use the design style that matches the type of design. The ability to create different parts of the same design using different paradigms, individually, or as part of a team, allows you to capture designs faster. At the heart of the Multi-Style Option is a spreadsheet-like interface to create design intent. Suitable for large pin-count devices and backplane designs, it also allows you to reuse existing subsets of the design created in schematics—power supply sections and analog/RF sections can be reused or integrated easily in the design.

The Multi-Style Option also allows multiple designers to work concurrently on a project. The intelligent design differences engine allows teams to simultaneously compare and reconcile changes when edits are made in logical and physi-

cal designs. The Multi-Style Option can be used throughout the design cycle, leveraging existing schematic symbols or no schematic symbols at all. The ability to include schematic blocks and use schematic libraries protects your current library investment. The Multi-Style Option also understands extended nets (Xnets), buses, and differential pairs, and it provides advanced features for handling terminations, pull-ups, pull-downs, and decoupling capacitors. It includes an online DRC engine, powerful reports, and schematic generation capabilities that make this a complete design solution for PCBs and packages.

Concurrent Team Design

Team design authoring enables multiple design engineers to collaborate asynchro¬nously in the hierarchical development of a logical design's definition. A design can be partitioned into user-defined levels of hierarchy and distributed to the defined members of the engineering team, provid¬ing them with an isolated "sandbox" for the development and verification of their partition(s).

The Allegro Design Authoring Team Design Option provides team assignment and notification capability to assign engineers to specific blocks they are going to author. It provides a dashboard view of the current status of each team member's block. This solution provides much-needed flexibility for large time-critical projects while accelerating the design creation process.

SKILL Programming

Engineers can write SKILL programs to customize Allegro Design Authoring and create custom commands. The custom programs can be used for querying and modifying the design data in schematic sheets. By placing these programs in a common area, it's possible for a team to share the efforts of all team members.

PDF Publishing

The Design Publisher Option converts Allegro Design Authoring schematics to content-rich Adobe Portable Document Format (PDF) files, creating a secure, single-file representation of the design. The PDF files provide navigation through the hierarchy as well as access to design attributes and constraints, making them ideal for design reviews. Intellectual property (IP) is protected through access controls that allow you to decide what design data is published for review.

Additional Utilities

Allegro Design Authoring provides additional tools that shorten the time to author designs:

- Part Manager tracks part usage to ensure that parts are always in sync with the design database

- Automatic Table of Contents (TOC) creation and management speeds schematic documentation

- Power pin signal assignment automates manual reassignment of power and ground connectivity commonly needed for large pin-count devices

- User-defined mouse strokes allow you to execute single or multiple commands directly from within the canvas without using the toolbar, menus, or console

- Function keys streamline design entry tasks by mapping complex or frequently used commands to a single key

Feature	Allegro Design Authoring
Flat, Hierarchical Schematic Creation	•
Page Navigation, Management, Hierarchy Viewer	•
Variant Editor	•
Project Manager	•
Cross Referencer	•
Archiver	•
Design Differences	•
Properties Worksheet, Differential Pair Worksheet	•
Support for Net Classes	•
User Customization	•
Part Manager	•
Bill-of-Materials Generator	•
Physical Design Reuse, Hierarchical Block Reuse	•
Import Blocks and Sheets	•
Copy Projects or Copy/Paste Within and Between Designs	•
Check Plus Rules Checker	•
Verilog and VHDL Netlisting	•
AMS Integration	•

Feature	Allegro Design Authoring
Build Physical Wizard for Xilinx, Actel, Altera	•
Customizable Menus, Custom Commands Using SKILL	•
Cross-Probing with PCB Editor	•
Electrical Constraints Sets	High-Speed Option
Physical, Spacing Constraints	High-Speed Option
Same Net Spacing	High-Speed Option
High-Speed Model Assignment	High-Speed Option
SigXp Topology Editor	High-Speed Option
Allegro Viewer Plus	High-Speed Option
Component Revision Manager	High-Speed Option
Manage Shared Area	Team Design Option
Assign, Notify Teams	Team Design Option
Dashboard View of Blocks in the Project	Team Design Option
Merge / Split Blocks	Team Design Option
Locking	Team Design Option
Out-of-Date Check	Team Design Option
Table / Spreadsheet-Based Design Creation	Multi-Style Option
Design Authoring Schematic Block Reuse	Multi-Style Option
Import Verilog Netlist from Existing Design	Multi-Style Option
Quick Connectivity Creation Functions	Multi-Style Option
Import Connectivity using Text Format	Multi-Style Option
Online Packaging	Multi-Style Option
Associated Components	Multi-Style Option
Schematic Generation for Multi-Style Designs	Multi-Style Option
Import Verilog	Multi-Style Option
Custom Reports	Multi-Style Option
TCL Support for Scripting and Extensions	Multi-Style Option
Route-Aware Automatic FPGA Pin Assignment	FPGA System Planner Option
Automatic Symbol, Schematic Creation for FPGA Sub-System	FPGA System Planner Option
Custom-Board ASIC Prototyping with FPGAs	FPGA ASIC Prototyping Option
Create and Publish Intelligent PDFs	Design Publisher Option

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customers realize silicon, SoCs, and complete systems efficiently and profitably. **www.cadence.com**